DFM AND SMT ASSEMBLY GUIDELINE

Revision	SCR No.	Description	Initial	Date
		Initial Release		8/3/21

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1 DFM Guideline Introduction

This document is intended to provide design criteria and process information that will promote automation, cost and cycle time reduction, and help to produce designs that will yield high quality forsolder attach of BKAV's SOM. The BKAV's SOM will be used in many assembly processes, and because all processes are different, this document provides a starting point, or "baseline" criteria application process development. This document is not intended to be the final process definition, nor is it intended to constrain designs. If customers cannot meet/follow all of the recommendations, they should contact BKAV to discuss the best alternatives.

1.1 Scope

This document discusses the BGA package and the main PCB immediately below the BGA. The guidelines do not cover all aspects of PCB design.

Since this is a rapidly evolving technology, spend some time reading recently published articles, papers, and company presentations on all aspects of fine-pitch PCB design.

A common theme emerged as this paper was developed – long standing "rules" for PCB design are no longer applicable at these small geometries.

The emergence of the theme came about as a result of many meetings among the different suppliers and designers. The meetings included representatives from four major team players of high yielding PoP design: PCB designers, PCB fabricators, component suppliers, and assembly vendors. Also, an extensive literature review was conducted and appropriate references are included at the end of this paper.

You should plan on performing your own experimental layouts and prototype runs before committing to volume production. Based on your findings, you'll discover that your suppliers can handle the device or you may have to change PCB fabricators and/or find assembly vendors with better equipment.

1.2 Purpose

The increasing focus on Design For Manufacturability (DFM) has resulted in expanding the scope of traditional design activities in order to identify and eliminate manufacturing problems during the design stage. DFM is as much a system as it is a task.

Although PCB design incurs only a small fraction of the total product cost, the decisions made during the PCB design phase determines the cost of the product over its life-cycle and can be crucial to the success or failure of the finished assembly.

In DFM all of the design goals and manufacturing constraints are considered simultaneously and analyzed. Such analysis can identify design elements that pose problems for manufacturing and suggest changes in the design to address these problems.

There are many ways to design a good PCB and the ideas presented here must be considered only as recommendations.

2 Levels of Requirement

Most PCB fabricators publish a table that indicates their limitations for various parameters like drill size, trace width, aspect ratio, etc. In many cases, these parameters may have more restrictive limitations when you consider other dependencies which result from one or two dominate characteristics of the PCB design. What this means is that there are tradeoffs and options for the PCB designer to consider. Always consult with your PCB fabricator for their limits and capabilities and remember that as you approach the limit of their equipment, yields go down and costs go up. As an example, we will describe a fabricator's technology and capabilities:

Standard Technology — Usually means this is the middle of the fabricator’s capability and pricing. The technology does not push the limits of the fabricator’s equipment. Our example fabricator may list a minimum trace width and clearance of 3 mils with 4 mil vias and 10 mil pads for standard technology.

High Yield Technology — Loosens up the specifications to provide more clearance and wider traces resulting in lower cost per unit PCB and higher yields. Our example fabricator may list a minimum trace width and minimum clearance of 4 mils with 4 mil vias and 10 mil pads for high yield technology. However, a PCB built using high yield technology may be larger and require more layers.

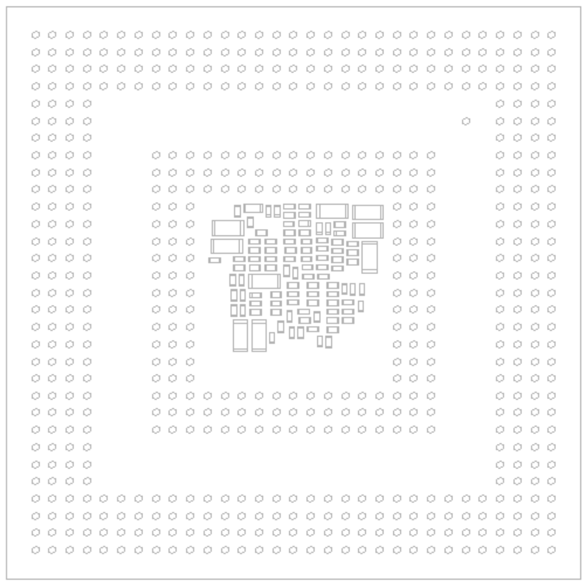
Engineering Development Technology — Really pushes the fabricator's capabilities to the limits of their equipment. Our example fabricator may list a minimum trace width and minimum clearance of 2.5 mils with 3 mil vias and 9 mil pads for engineering development technology. Do not make the mistake of thinking these limits can be used for production. The cost will be high and the yield may not be good.

For each requirement, an impact and benefit statement is included to quantify the requirement. Some requirements are stated as being recommend or preferred per the following:

Recommend:	The minimum processing requirement – a deviation will most likely impact manufacturability and cost.
Preferred:	Should be done when possible – a diviation could impact manufacturability and cost.

3 Design Introduction – BKAV’s SOM

Top View


Bottom View

The BKAV’s SOM is organized in LGA package which accomodates 601 possitions as side picture.

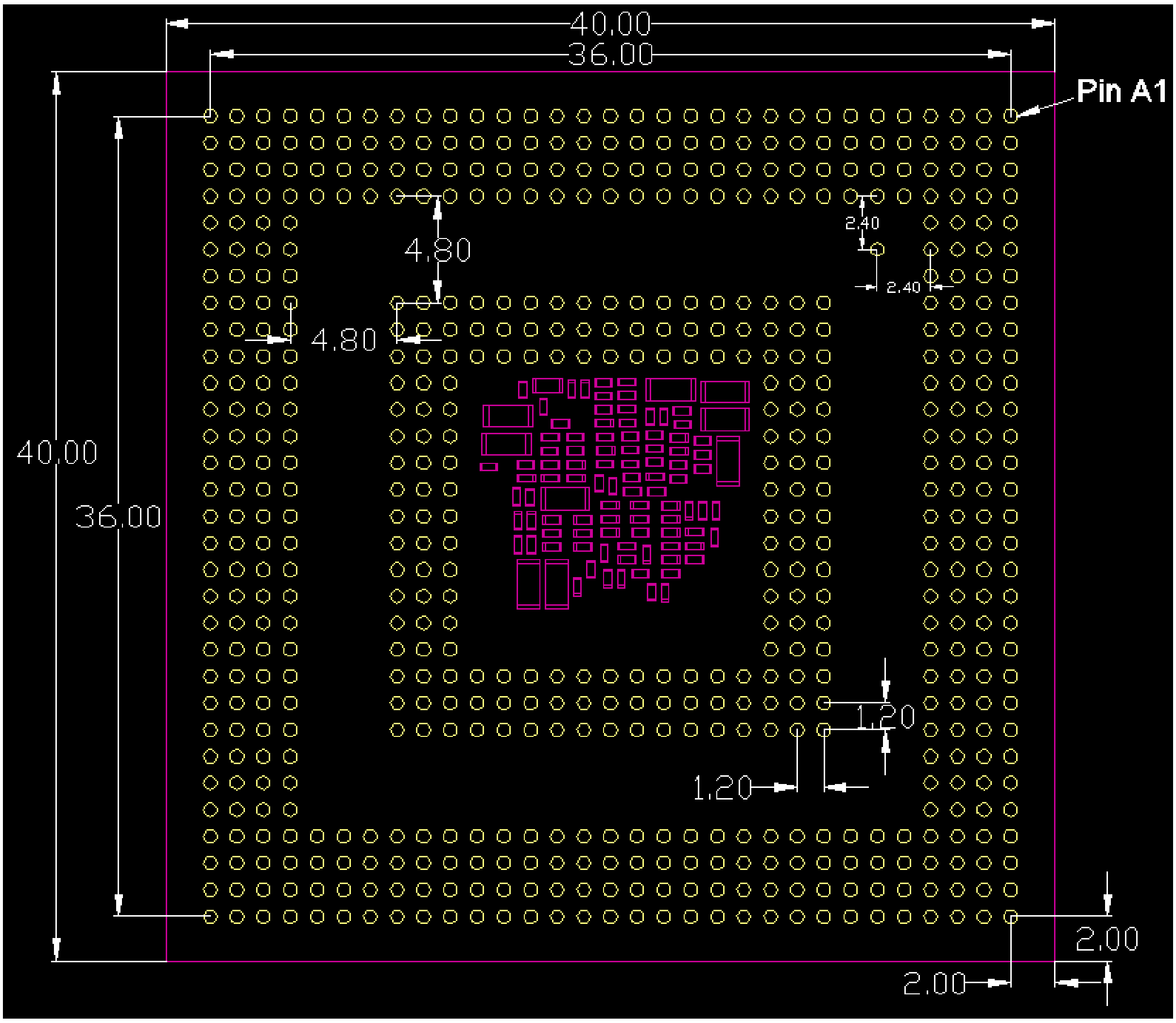
Some benefits of the LGA package over a BGA package include:

- LGA devices can be used for either lead containing or lead-free assemblies depending on the surface mount technology (SMT) assembly solder pasted used.
- LGA eliminates risk that customers receive components with missing or damaged spheres dueshipping or handling.
- LGA devices have a lower mounted height than BGA. This can allow for more space above the device for a heat sink solution or for small form-factor applications.
- Board-level reliability significantly exceeds customer requirements when the design and process recommendations are followed.

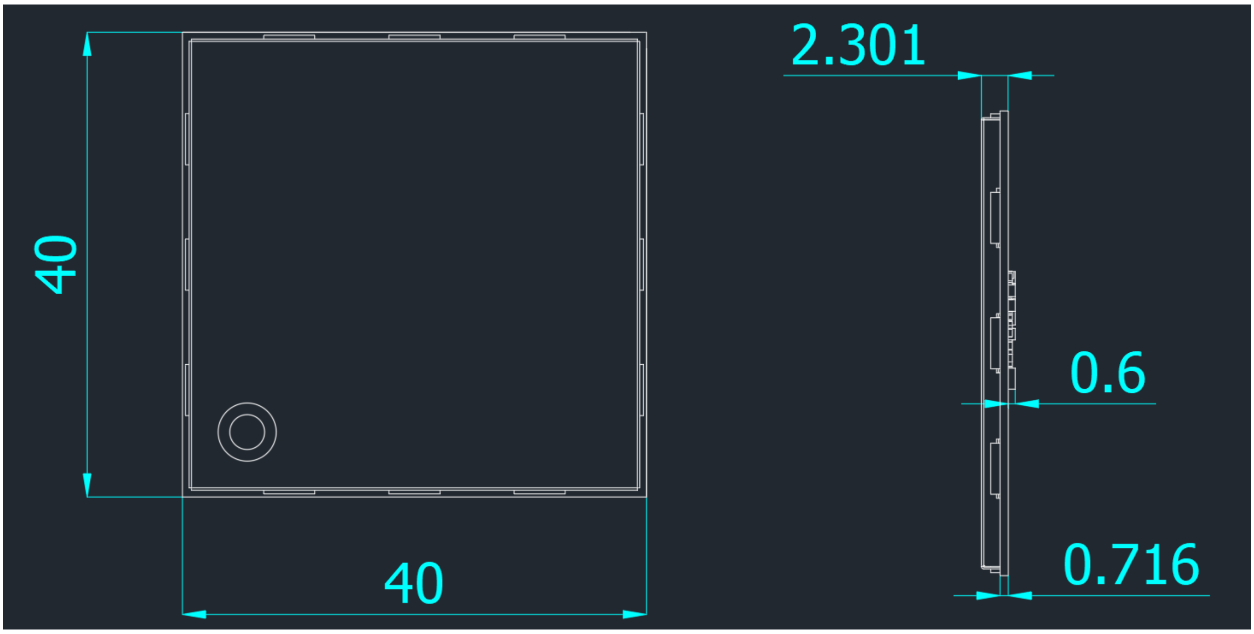
- The durability of LGA in mechanical drop is typically greater than a BGA that is not underfilled.
- LGA can use the same recommended board assembly process as CBGA.

4 SOM Package

See detailed Package Dimension as below:



Bottom View (dimension: mm)



5 Routing and Layer Stackup

One huge benefit of PoP is the elimination of the high-speed, balanced transmission lines between the processor and memory. The external memory's data and control lines no longer have to be routed out from under the processor. This is a huge savings in both time and the number of layers. For these reasons, OEMs have quickly adopted PoP as their applications processor package of choice. This also impacts your pad and layer stackup decisions.

A customer does not need to worry about PCB design requirements for external high-speed DDR memory when using PoP because this interconnect is not part of the main PCB design.

It is possible to use a 6-layer PCB and route all of the connections without requiring via in pad technology. There are several suitable layer stackups.

If the stackup above is used, great care must be taken to minimize cross talk between the outside 2 layers on both the top and the bottom. Also, signals must still adhere to the impedance recommended in the respective component data sheet (45-65 ohms in most cases), so care must be taken to allow the traces to have a reference plane for impedance control.

Layer 1	Signal (Top Copper)
Layer 2	Signal
Layer 3	Ground
Layer 4	Power
Layer 5	Signal
Layer 6	Signal (Bottom Copper)

Another popular stackup, shown below, allows for sensitive clock signals or relatively high-speed lines to be routed between power planes.

Layer 1	Signal (Top Copper)
Layer 2	Ground
Layer 3	Signal - high speed
Layer 4	Signal - high speed
Layer 5	Power
Layer 6	Signal (Bottom Copper)

Another recommended stackup.

Layer 1	Ground with pad cutouts
Layer 1	Signal – high speed
Layer 3	Signal - high speed
Layer 4	Power
Layer 5	Ground
Layer 6	Signal (Bottom Copper)

At first it would seem that using ground as the top layer would not be efficient. Once the designer realizes that this reduces vias by ~30% (because of the number of pins connected directly to ground) and therefore promotes great routing efficiency on the second layer, the advantage is seen. Several high-density interconnect (HDI) experts have used ground as the top layer and recommend this practice. This stackup also provides reduced EMI.

In addition to layer stackups, package footprints and pad stacks are the next important item to consider. Proper definitions and strict adherence to clearance will play a key role in the development of high yield PoP designs.

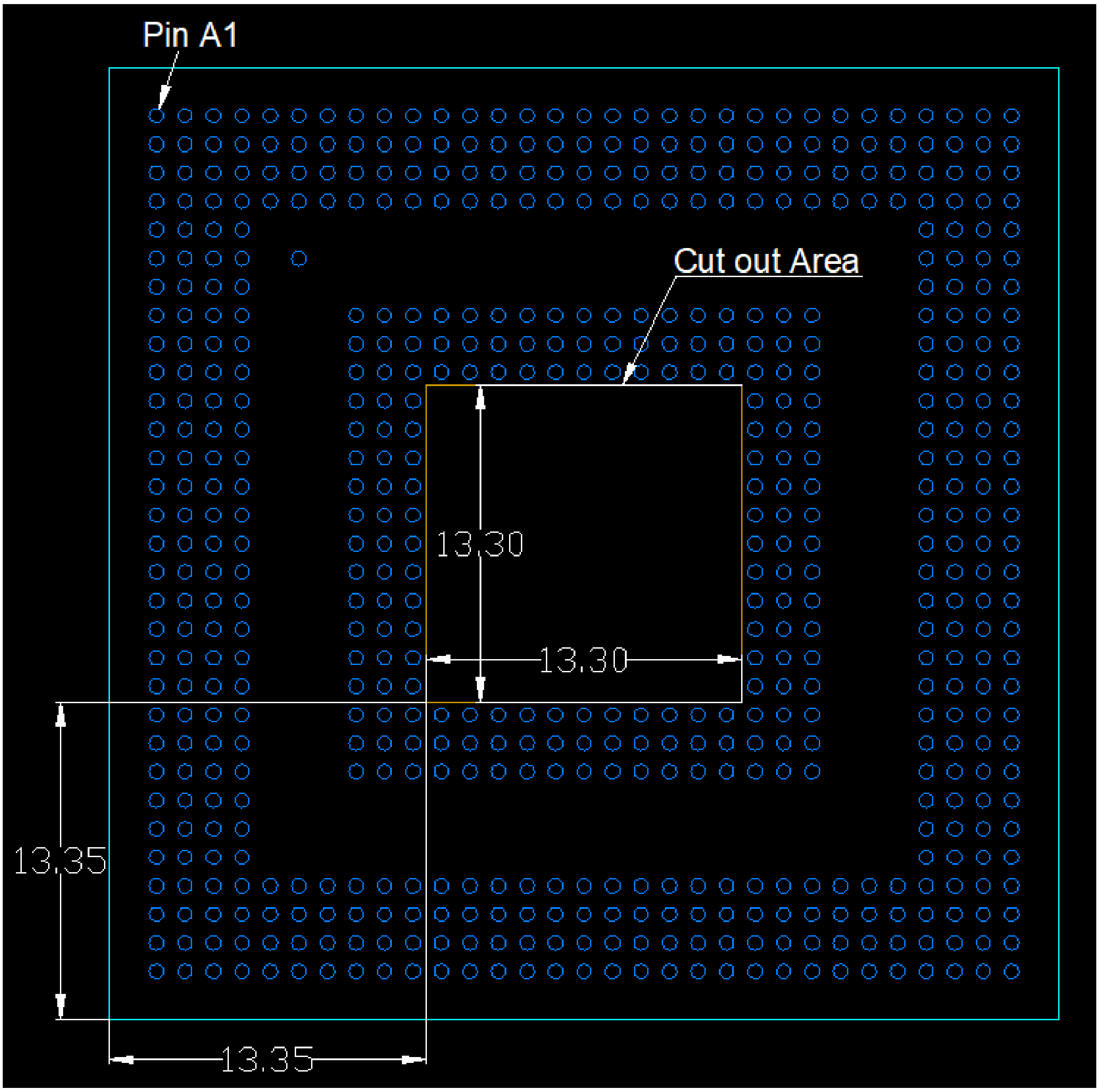
6 PCB Design

The recommendations made below have a direct impact on the reliability of the solder joint and play an important role in facilitating the SOM's ability to self-center and achieve the best possible location tolerances.

Requirements	DFM Impact/Benefit

• Recommend using a "Copper Defined" landing pad as opposed to a "Solder- Mask Defined" pad.	• "Copper defined" better insures a round, accurately located pad – critical to part location tolerance. • "Copper defined" pad produces a more reliable solder joint – allowing solder to wrap around the pad edge.
• Pad Size = .60mm (.024")	• Smaller pad will result in decreased ball-to-pad angle, based on solder volume – increasing the risk of solder fracture. • Larger pads will increase the risk of shorting.
• Solder mask should be clear around pad	• In-accurate registration will result in solder mask encroaching onto copper pad.

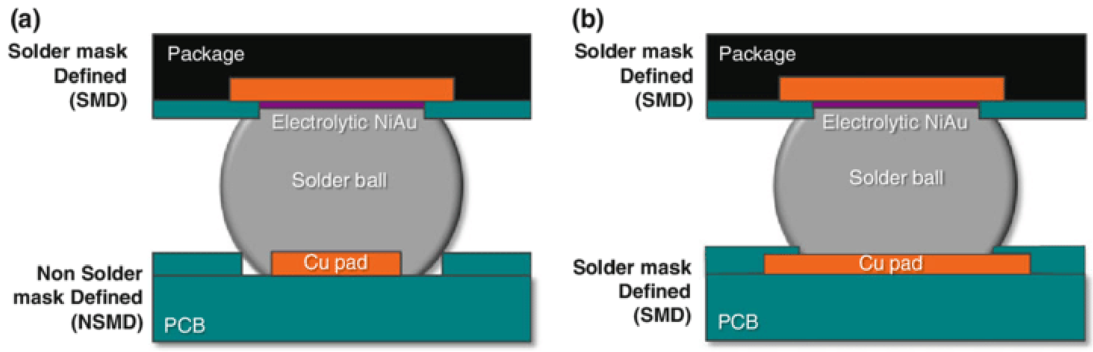
6.1 Recommend Land Pattern



Top View

6.2 PAD TYPE

Before getting into the specific details, it is important to understand the pros, cons, and unknowns concerning the two most common types of solder pads, solder-mask-defined (SMD) and non-solder-mask-defined (NSMD) pads.



We are recommended use NSMD pads to design PCB for SOM. They have the advantage of tighter copper dimensions, compared to solder mask dimensions, and the uniform coverage is better at the solder melting temperature. The pads are also smaller, allowing for improved routing. Another advantage of the NSMD pad is reduced stress concentrated on the solder joint, which increases solder joint reliability especially if paste overprinting is used. This concept will be covered later in a section that discusses solder stencil design.

However, there are some companies that swear by SMD pads claiming that the greater copper area (of the pad) and the solder-mask overlap create better adhesion strength to the fiber/glass laminate. They claim that flexing and bending during accelerated thermal cycling testing causes a weak link where the pad attaches to the PCB and could be the main failure location, as opposed to the typical solder fracture which dominates the NSMD pad.

Be sure and talk to your PCB fabricator and your PCB assembly vendor and discuss their experiences and preferences before deciding which type of pad will be used on your PCB design.

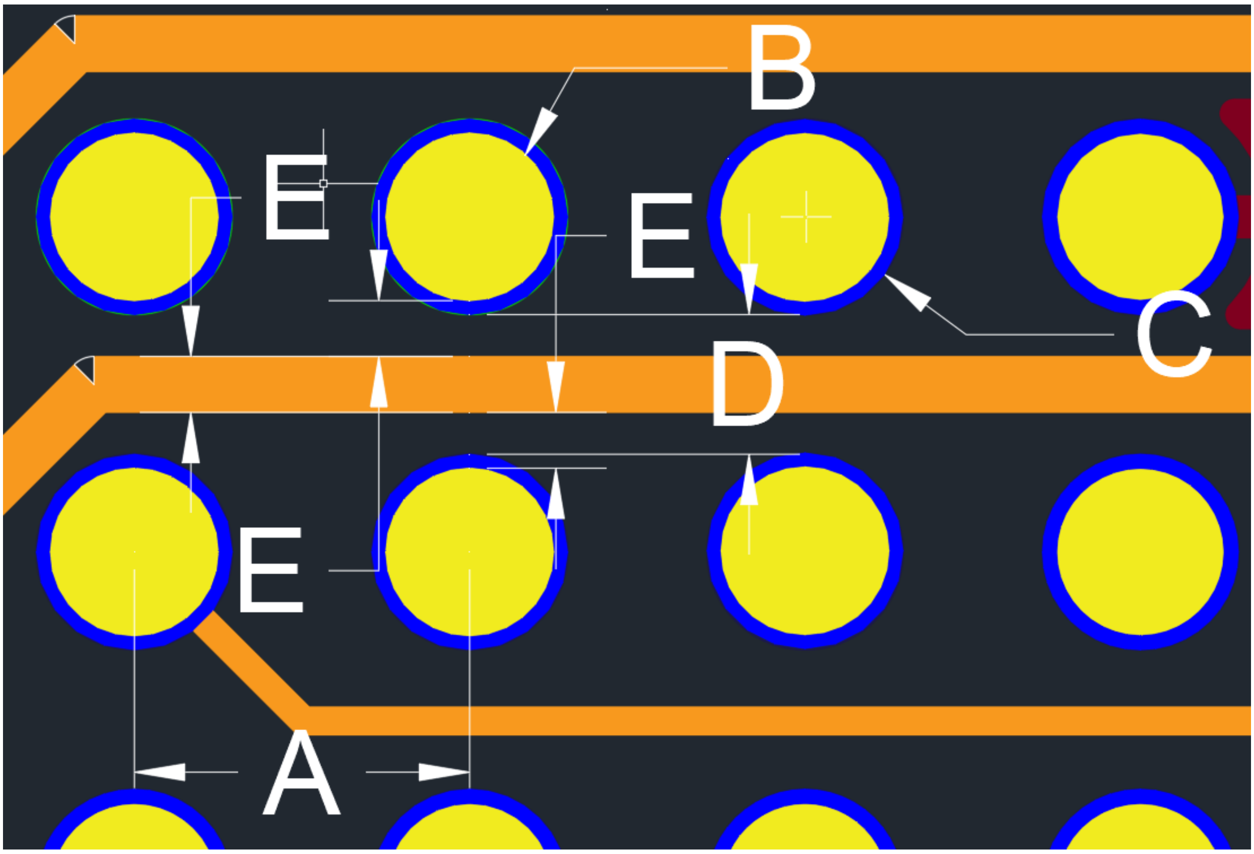
6.3 PCB Dimensions for 1.2mm pitch with routing track

Through several meetings with both PCB fabricators and PCB assembly vendors, the following recommendation has been created for the PCB LGA footprint. The pattern shown in Figure below assumes there will be traces between solder pads on the top layer.

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad according to several industry studies. In addition, there is additional “grip” area around pad edge as previously described.

Finally, the suggested clearance around the pad for the solder mask opening is about 50um (2mil).

Pad Type	NSMD	
Pad Pitch	A	1.2mm
Pad Size	B	0.6mm
Mask Shape	Round	
Mask Opening	C	0.05mm around pad (0.7mm antipad for the 0.6mm pad)
Mask Web	D	0.6 mm
Trace Allowed Between	Yes	
Trace Width	E	0.2mm
Pad to Trace Clearance	E	0.2 mm

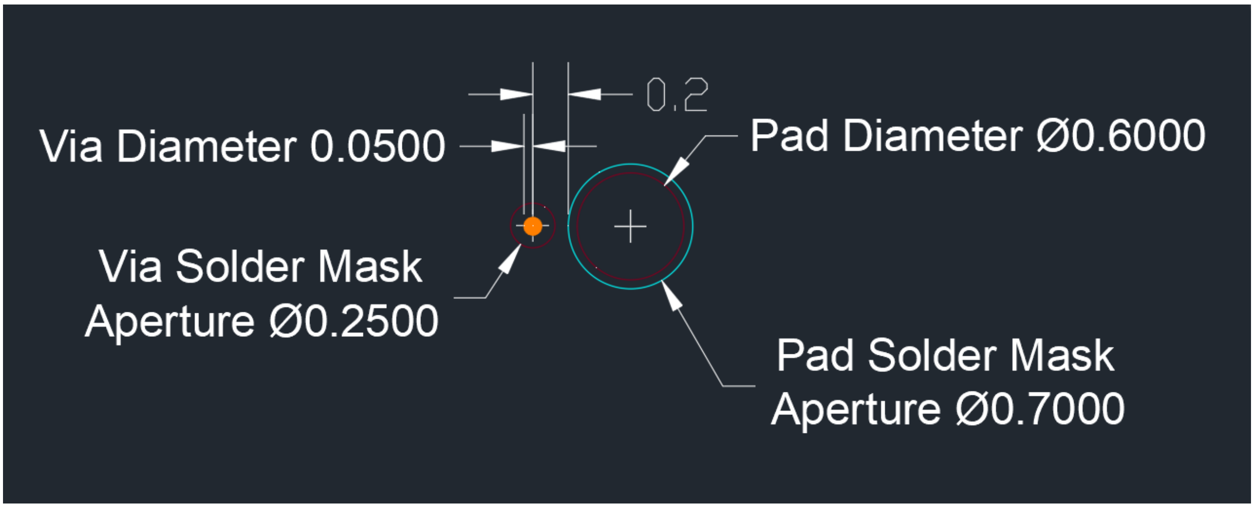


6.4 PCB Dimensions for 1.2mm pitch with via

When you want to use vias to drop down to lower layers, the following technique is commonly used. At the 1.2mm pitch, there is sufficient space between pads to allow for a via that has the same dimension as the package pad. The pad and via are connected with a 200um wide trace. The pattern shown in Figure below shows how vias are used to connect solder pads on the top layer to subsequent layers.

This type of via is referred to as an “offset via” and is very robust. Note that the via is completely covered by the solder mask. This prevents short circuits during paste application, allows for paste overprinting (discussed later) and prevents etch entrapment.

Pad Type	NSMD
Pad Pitch	1.2mm
Pad Size	0.6mm
Via pad size	0.25mm
Via drill size	0.1mm
Pad to Via clearance	0.175mm
Pad to Via Trace	0.2mm wide



6.5 Teadrops and snowman pad

Teardrops should be used when traces exit the pad whether it is a solid pad or a pad with a via. One way of creating teardrops is to add secondary pads at the junction of an existing (primary) pad and the trace, sometimes called a "snowman." These secondary pads are sized 0.05mm smaller than the primary pads, and the center is placed 0.075mm away from the center of the primary pad.

This technique is designed to provide additional metal at the critical junction of a pad and a trace. It becomes especially important during the process of registration and via drilling. This will reduce solder joint stresses, reduces risk of cracking, improves resistance to thermal shock and improves resistance to impact shearing. Use of teardrops, in conjunction with NSMD pads, provides additional ball-to-land contact area, making them more mechanically robust.

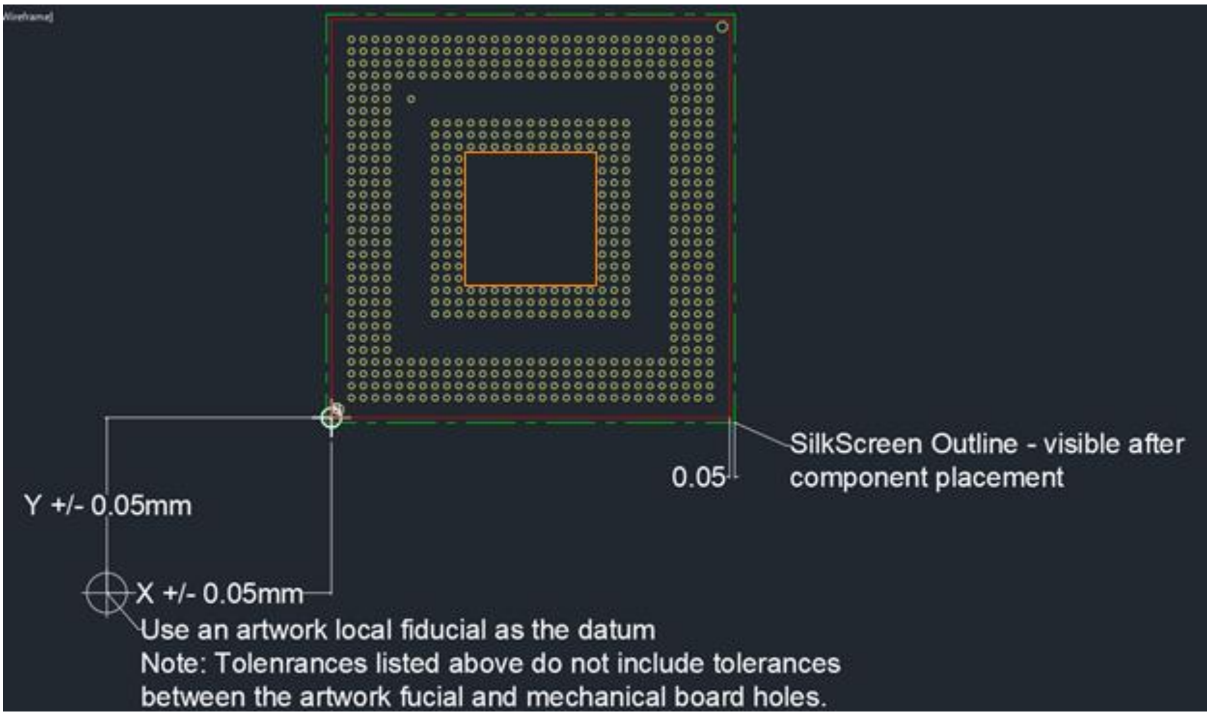
Check the latest IPC standards and discuss them with your PCB fabricator and PCB designer. In some cases, this feature is simply a check box on your CAD system or something that your PCB designer will do for you.

6.6 PCB Assembly guideline

The BKAV's SOM is designed to accommodate SMT assembly and PCB fabrication tolerances. Below are the total allowances for the SOM design, and the recommended PCB fabrication tolerances.

Spec: Max Allowable X Array shift +/-0.05mm

Max Allowable Y Array shift +/-0.05mm



6.7 Keep-out zone and clearances

The BKAV's SOM keep-out zone is required for re-work capability. This allows clearance around the connector housing for rework tooling and nozzles.

Requirements	DFM Impact/Benefit
• Depend on the dimension of your designed board, clearance between SOM and another parts can be adjusted. The recommended minimum clearance	• Rework nozzle - physical clearance

required is 0.25mm – preferred clearance is 0.4mm to non-fragile adjacent components.	
• It's preferred to have 0.5mm clearance to adjacent devices that are very fine pitch with small thermal mass, and could reflow – this is dependent on board thickness, and copper weight	• Prevents reflow of adjacent device, which could cause shorts/defects on that device.

6.8 Device handling

Requirements	DFM Impact/Benefit
• SOM should be kept in the original packaging until they're used.	•Protects the land pad field until it can be loaded into the placement machine
•It is not necessary to bag and re-vacuum seal* the tray, if the parts are used within a reasonable time frame for eutectic solder balls – shelf life is dependent on stockroom environmental conditions.	•BKAV's SOM materials are not moisture sensitive, and do not require pre-bake.
•Place tray flat on rack for storage or transport – don't place on edge.	•Prevents parts from moving out of tray slot.

6.9 Solder paste process

Requirements	DFM Impact/Benefit
•Liquid Photo-Imageable (LPI) solder mask over bare copper is preferred.	• Most common – provides best adhesion for solder mask - preventing peeling and flaking of mask during assembly processes.
•Preferred to use a 6 mil stencil (Minimum stencil thickness of 5 mil)*	• Minimizes the risk of opens
•Recommended to use a reduced aperture - .021”	• Minimizes the risk of shorting

*A 5mil stencil thickness can be used, but requires either a .005”/inch board warp spec, or a .001” pad co planarity spec on surface finish thickness variability. (HASL finishes can exceed this limitation.)

Board Warp Matrix - The following matrix defines the board warp spec required for each of the listed variables – Stencil Thickness and Pad Finish Co-planarity.

		Pad Finish	Co-planarity
		<.001”	<.002”
Stencil Thickness and	5 mil +2/-0 mil	0.007”	0.005”
	5 mil +2/-.5 mil	0.005”	Not Recommended

Paste Process Variation	6 mil +2/-0 mils	0.007”	0.007”
	6 mil +2/-.5 mil	0.007”	0.005”

6.10 Placement process

This range of connector heights fall within the 0-1/2” range of focal length – most common placement machine capabilities. (Note: if customers placement equipment standard height range is less than 1⁄2” – refer to section below for more info.)

Requirements	DFM Impact/Benefit
• “All-pin” field alignment is preferred	• Most accurate placement
• Housing align, back-lit black-body align, or mechanical align not recommended	• Plastic housing to ball field tolerance stack-up will result in less than optimal placement accuracy
• Full circular side lighting is preferred – see below	• Ability to most accurately find the ball, without background lighting issues.
• Product should be pre-oriented for machine vision system alignment.	• Prevents nozzle slip/skew, between camera and placement, due to weight of SOM.

• Placement location/centroid of the part should be based on the ball locations, and placed using a best-fit alignment	• Minimizes the percentage of foot-print that is off-pad.

*Note: Set-up should be verified for placement repeatability and accuracy. Contact BKAV for information on verification tools.

6.11 Placement process – feeders

Requirements	DFM Impact/Benefit
• SOM are shipped in standard JEDEC outline trays and are equipped with a cap that provides a flat vacuum surface – see below and next page.	• Meets the requirements of industry standard placement equipment
• Trays should be loaded into machine with the "tray-notch" in the upper left hand corner - for both the plug and receptacles. See diagram next page.	• Allows for part set-up standardization across the product line. • Consistent loading of all parts minimizes the risk of reversed loading of the tray into the placement machine.

6.12 Reflow process

Requirements	DFM Impact/Benefit

• To determine correct oven settings, follow standard reflow profile processes for set-up and placement of thermal probes.	•Insure even heat distribution across the part.
• Locate one thermal probe on top of the connector housing during reflow profiling – It is preferred to keep the plastic below 260°C with a max allowable temperature of 280°C.	•Insures against plastic over-heating and damage.
• Set process to the solder paste vendor’s recommended profile.	•This varies by the chemical make-up of each solder paste, and also varies from one paste vendor to the next.

6.13 Rework process

The rework of a BKAV’s SOM, for solder shorts and opens, requires that the SOM be completely removed and replaced with a new SOM.

Requirements	DFM Impact/Benefit
• Use specialized BGA rework equipment for connector removal and replacement, and should include thermal profiling and temperature measurement capability.	•Achieves an all-footprint reflow at point of removal without excessive heat to the connector and PCB, or insufficient heat causing lifted pads.

• Locate one thermal probe on top of the connector housing during reflow profiling – It is preferred to keep the plastic below 260°C with a max allowable temperature of 280°C.	•Insures against plastic over-heating and damage. (See reflow section for more detail.)
• Placement location/centroid of the part should be based on the footprint locations, and placed using a best-fit alignment	• Minimizes the percentage of footprint that is off-pad.
• Semi-Automated placement capability is preferred – including vacuum pick-up and placement.	• This will provide consistent placements.
• Split Vision alignment systems are required to allow a ball-field best-fit alignment to PCB footprint.	• Allows blind alignment of footprint to pad - minimizing placement error.
• Hand/Manual placement is not recommended.	• Manual placement is inconsistent, and blind/housing align does not provide the required placement accuracy.
• Follow normal rework processes for PCB site cleaning and prep, and reflow profile development.	• Improves rework yield and insures reliable solder joints
• “Flux-only” processing is not recommended.	• Inconsistent amount of metal left on pad during site prep, resulting in

	excessive pad co-planarity variation – increased risk of solder opens.
• Paste deposition is recommended using either an automated dispensing system or manual micro stencils – resulting in a 6 mil tall x 21 mil diameter deposit.	• Prevents opens/shorts with high reliability solder joints.

7 Reference

1. NexLev DFM and SMT Guideline
2. Design for Manufacturability (DFM) Design for Assembly (DFA) - Joe Belmonte
3. InfinX DFM and SMT Guideline