K200 OPEN DEVELOPMENT KIT

Hardware User Guide

Rev.A

May 18, 2021

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1 K200 Open Development Kit

Powered by the Qualcomm® Snapdragon™ QCS605 SoC (System on Chip) also known as the Qualcomm® Vision Intelligence Platform, the K200 ODK is the perfect reference design for the AIoT camera. By combining the Qualcomm® Artificial Intelligence Engine with our industry expertise in imaging products, you are guaranteed the best-in-class product for your edge computing needs.

1.1 Key feature

Component	Description
SoC	• Qualcomm QCS605 processor
CPU	• Custom 64-bit ARM v8-compliant octa-core CPU • Up to 2.5 GHz,10nm process technology
GPU	• Qualcomm Adreno 615 GPU • OpenGL ES 3.2, Vulkan, DX 12.x • OpenCL 2.x, Microsoft DirectCompute, RenderScript
DSP	• Qualcomm Hexagon V65 DSP
RAM	• 2GB LPDDR4x SDRAM @ 1866 MHz
Storage	• 16 GB eMMC 5.1 onboard storage • 1 x MicroSD card slot

Ethernet	• 1 x GbE Ethernet
Wireless	• WLAN 802.11 a/b/n/ac 2.4/5GHz 2x2 MIMO • Bluetooth 5.0
GPS	• GPS/GLONASS
USB	• 1 x USB 3.1 Type C
Display	• Two, 4-lane DSI D-PHY 1.2 or C-PHY 1.0; VESA DSC 1.1 • 1 x HDMI 1.4 (Type D - full) connector
Video	• Encode: 5.7K30/4K60 8-bit: HEVC/H.264 + 1080P60 • Decode: 5.7K30/4K60 10-bit: HEVC/VP9/H.264, HDR 10
Audio	• AAC, PCM playback/record • Stereo encoder
Camera	• 2x ISP 14 bit + 1x Lite ISP: 32 MP (2x ISP, 16 + 16 MP) • 16 + 16 IFEs, DxO 90, SHDR, MCTF, fisheye dewarping, EIS
Expansion interfaces	Expansion connectors: • J0809: 1 x 16 pin high-speed connector (4L- MIPI DSI1) • J0901: 1 x 50 pin high-speed connector (4L-MIPI CSI0, CAM MCLK x 1, GPIO x 11, I2C x 1, DC Power) • J0807: 1 x 16 pin high-speed connector (4L - MIPI CSI1)

	• J0806: 1 x 16 pin high-speed connector (4L - MIPI CSI2) • J0805: 1 x 30 pin low-speed connector (LPI GPIO x 16, UART, I2C x 1, GPIO x 7, DC Power) • J0808: 1 x 30 pin low-speed connector (PMIC power on x 28, GPIO x 2) • J0803: 1 x 8 pin low-speed connector (JTAG x 6, GPIO x 1, DC Power) • J0801: 1 x 12 pin low-speed connector (LPI GPIO x 6, GPIO x 2, Audio codec x 4) • J0804: 1 x 6 pin low-speed connector (ALARM IN x 2, ALARM OUT x 1)
LED	3 Indicator LED • 1 LED for Power Indicator • 2 LED for LAN Ethernet block
Buttons	• Power (on/off/reset)
Power source	• 12V - 1A adapter with a DC plug (5.5x2.1mm) • PoE 802.3at/af with a RJ45 plug
OS support	• Android-based • CC SDK – Framework QMMF for recording and playback
Size	• 101mm x 68 mm

1.2 Board view

1.2.1 Top view

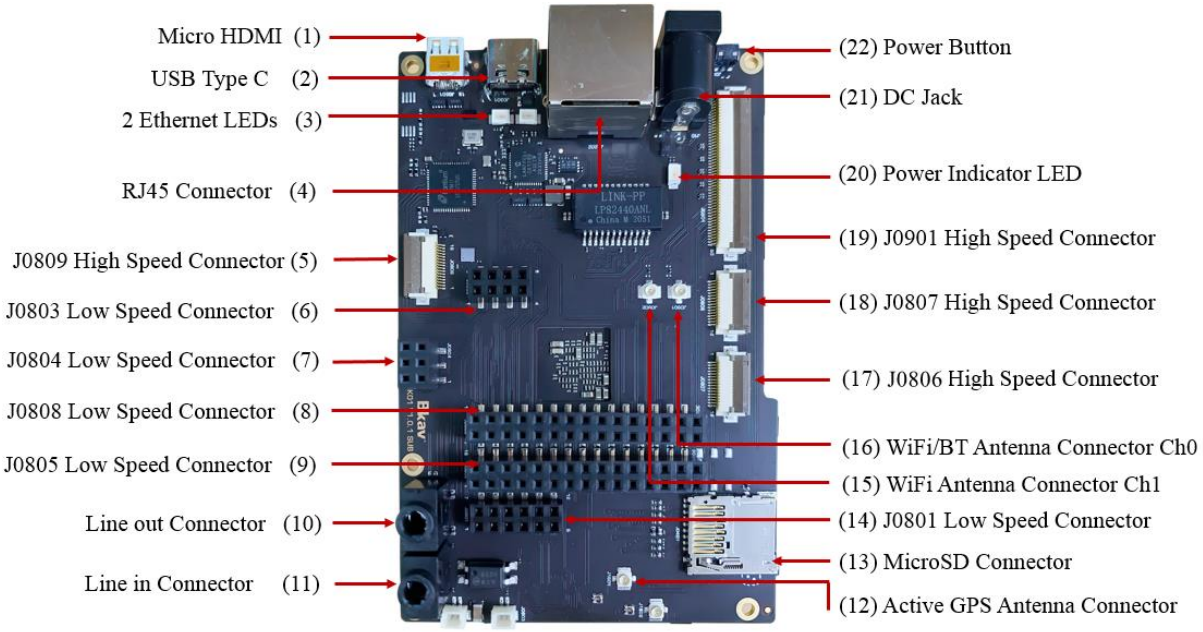

Figure 1. Board Top view

1.2.2 Bottom view

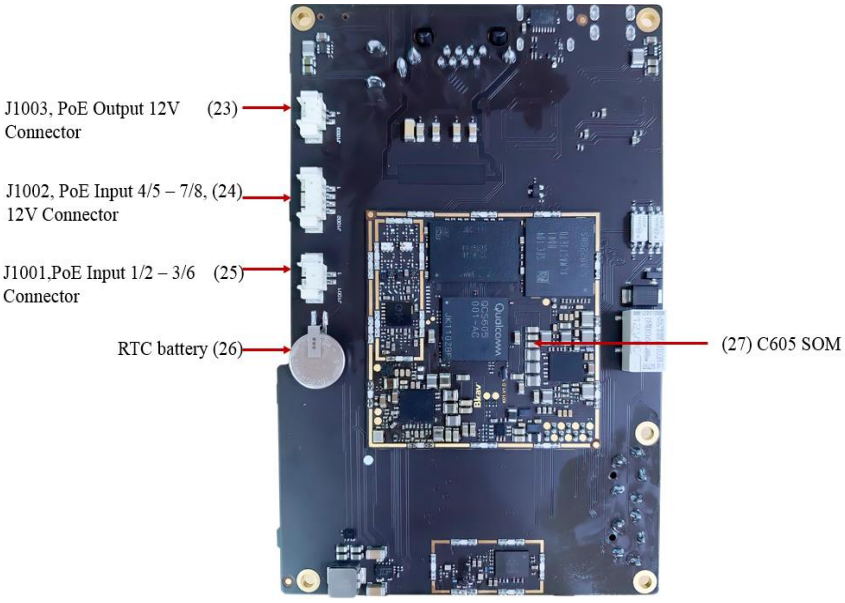

Figure 2. Board Bottom view

1.3 Box content

The box contains one K200 development board and accessories are:

- One 12V-1A adapter
- One active GPS antenna
- Two Wifi antennas

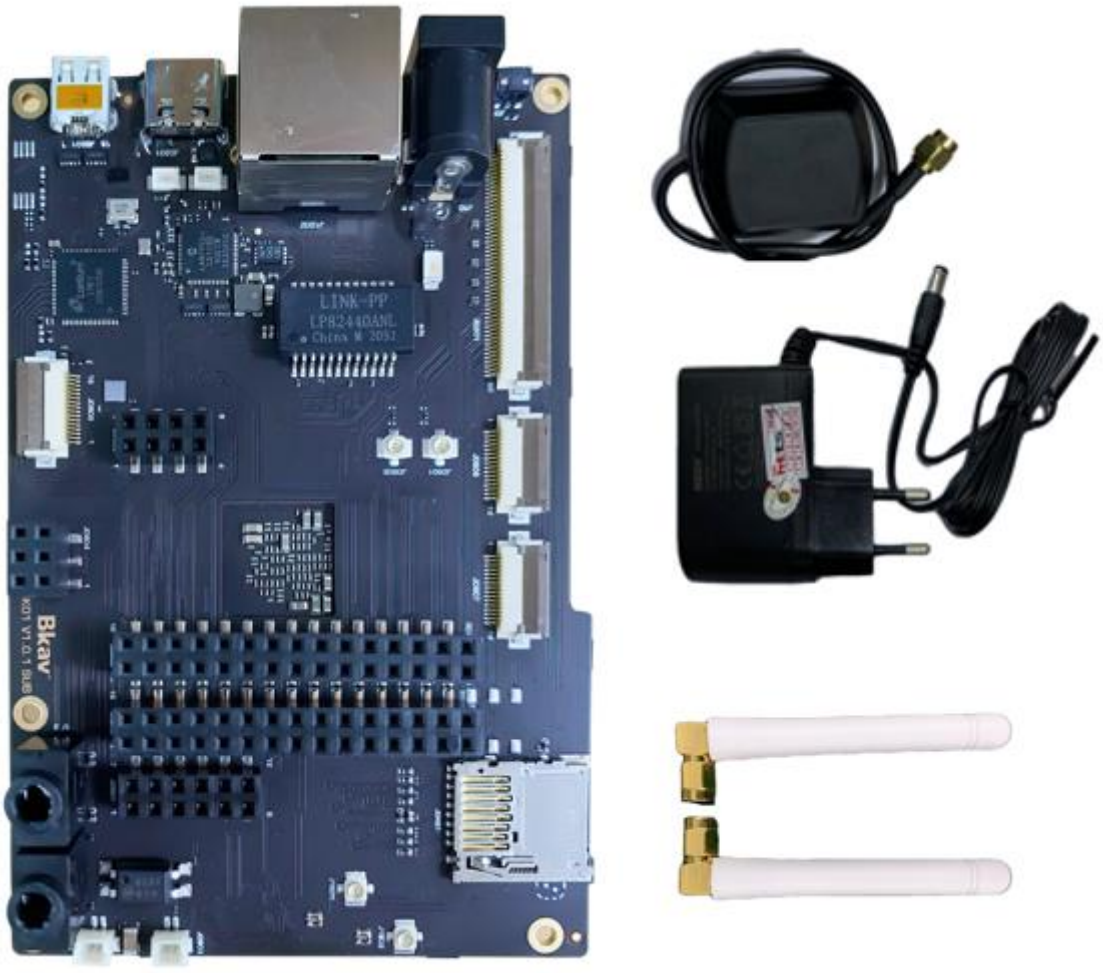

Figure 3. Box content

1.4 Terms and Definitions

Abbreviations	Description
QUP	Qualcomm Universal Peripheral The QUP engine provides a general-purpose data path that supports multiple mini cores, e.g., UART, I2C and SPI
ODK	Open Development Kit

2 Start the board

2.1 Required equipment

Equipment	Description
The evaluation board	Based on the Qualcomm® QCS605 processor
Power adapter Or PoE PSE	12V-1A 802.3at/af standard
USB to COM Module	For serial console interface and ADB, Fastboot commands
USB to USB Type C cable	For connecting the USB 3.1 Type C port and flashing images
Host PC	For connecting the board and installing Fastboot

2.2 Android OS startup process

Step 1: Connect the power supply by 12V adapter or PoE-Injector/ PoE Switch to power connector (see Section 1.2.1, #21), RJ45 connector (see Section 1.2.1, #4) respectively

Step 2: Plug the power supply into a power outlet. The green power-up LED (see Section 1.2.1, #20) should illuminate.

Step 3: Press and release the power button on the device (see Section 1.2.1, #22) or connect USB to USB Type C cable from PC to connector (see Section 1.2.1, #2). The board will start the booting process.

Note: For getting log on booting process, can use the serial console tool on the host PC For example: Minicom, Refer as below to connect the host PC and board.

Step1: Prepare a module USB to COM, example FT232.

Step2: Connect RX, TX, GND signal in module USB to COM to pin 20, 21, 29 of connector J0805 (see Section 1.2.1, #9) respectively.

3 K200 development board

3.1 System block diagram

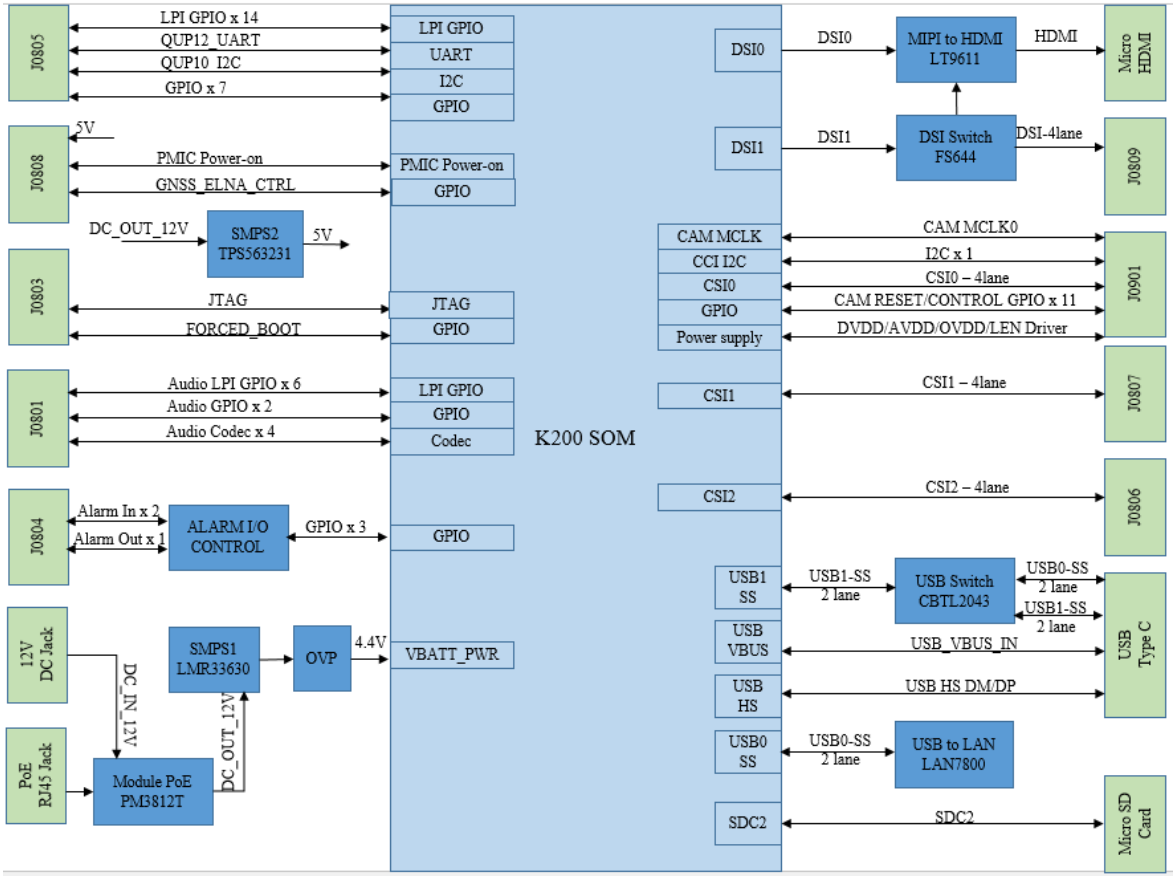

Figure 4. System block diagram

3.2 Processor

The QCS605 processor features a 64-bit ARM v8-compliant octa-core Qualcomm® Kryo™ 300 CPU. The processor supports LPDDR4X SDRAM interface, compute DSP with Qualcomm® Hexagon™ Vector eXtensions, 32MP camera, Qualcomm® Adreno™ GPU, 4K video encode and decode, and Bluetooth 5.0.

3.3 Memory

The QCS605 board uses a LPDDR4X RAM and eMMC 5.1 flash memory discrete.

- LPDDR4X interfaces directly to the QCS605 built-in LPDDR controller. The maximum DDR clock is 1866 MHz
- eMMC flash memory interfaces with the QCS605 processor over a dedicated eMMC PHY bus supporting the eMMC 5.1 specification.

3.4 MicroSD

The QCS605 microSD slot (see Section 1.2.1, #13) signals are routed directly to the QCS605 SDC2 interface.

The slot is a push-push type with dedicated support for card detect signal (many microSD slots do not have dedicated CD pins, they use DATA3 state as the card detect signal). The QCS605 board uses GPIO_96 as the SD_CARD_DET_N.

3.5 WiFi and Bluetooth RF

The QCS605 board uses the Qualcomm RF chip WCN3990 solution that integrates two wireless connectivity technologies into a single device.

The technologies are:

- WLAN-compliant with IEEE 802.11 b/g/n/ac specifications
- Bluetooth-compliant with the BT specification version 5.0 (BR/EDT + BLE).

The K200 Sub board Antenna Socket #16 (see Section 1.2.1) for WiFi chain 0 (and optionally BT) is connected with external WiFi Antenna.

The K200 Sub board Antenna Socket #15 (see Section 1.2.1) for WiFi chain 1 is connected with external WiFi Antenna

3.6 GPS

The QCS605 board uses the Qualcomm RF chip SDR660G solution that integrates GNSS connectivity technologies.

The K200 Sub board Antenna Socket #12 (see Section 1.2.1) for Active GPS Antenna.

3.7 Display interface

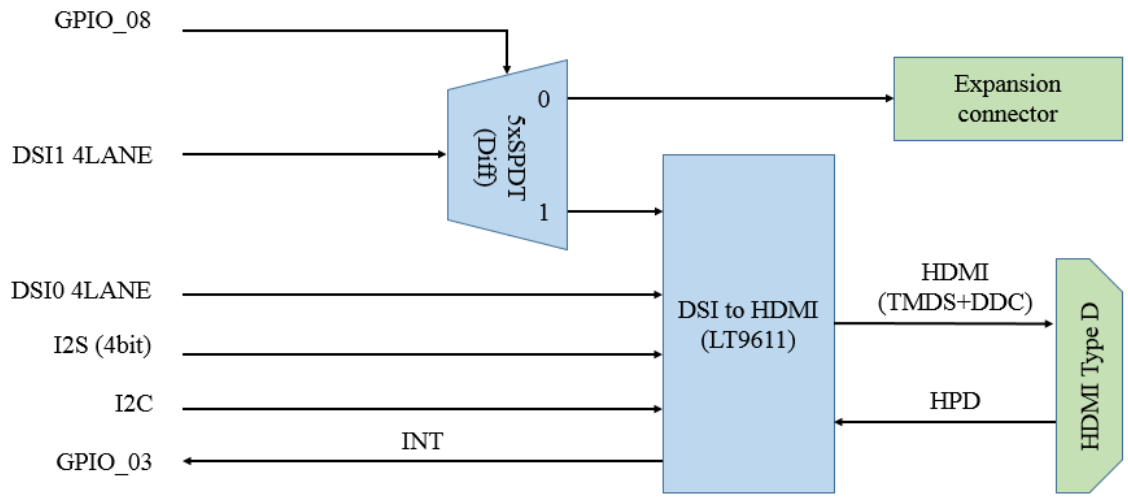

Figure 5. Display interface

3.7.1 HDMI

The QCS605 processor does not include a built-in HDMI interface.

The SUB board deploys the built-in MIPI-DSI 2x4 lanes interface as the source for HDMI output. A peripheral DSI to HDMI bridge (LONTIUM SEMICONDUCTOR LT961) performs this task and supports a resolution from 1080p to 4K at 30 Hz. While the LT9611 supports automatic input video format timing detection (D-PHY1.2, DSI1.3/CSI-2 1.00 and DCS 1.02.00), an I2C channel from the QCS605 processor allows the user to configure the operation of this bridge. The QUP0 I2C interface from the SoC connects to the bridge. This bridge supports audio as well. The SUB board uses a 4-bit I2S2 interface from the QCS605 processor for this task.

As required in the specification, a MIPI-DSI interface is routed to the high-speed expansion connector. Since the QCS605 processor has two MIPI-DSI interfaces for HDMI, a muxing device (FSA644UCX) is used on the board. Only one interface, HDMI, or the expansion MIPI-DSI can be active at a given time. The controlling signal is named QCS605_GPIO_8. When this signal is logic high, 1, the MIPI-DSI is routed

to the DSI-HDMI bridge. When QCS605_GPIO_8 is logic level low, 0, the MIPI-DSI is routed to the high-speed expansion connector. This design assign the QCS605_GPIO_8 function to GPIO_8.

3.7.2 MIPI-DSI

The K200 Sub board has a 4-lane MIPI_DSI interface meeting this requirement. See Chapter 5 for details.

3.8 Camera interface

The K200 Sub board has three camera interfaces.

- 4-lane CSI0 camera on J0901 connector
- 4-lane CSI1 camera on J0807 connector
- 4-lane CSI2 camera on J0806 connector

3.9 USB Port

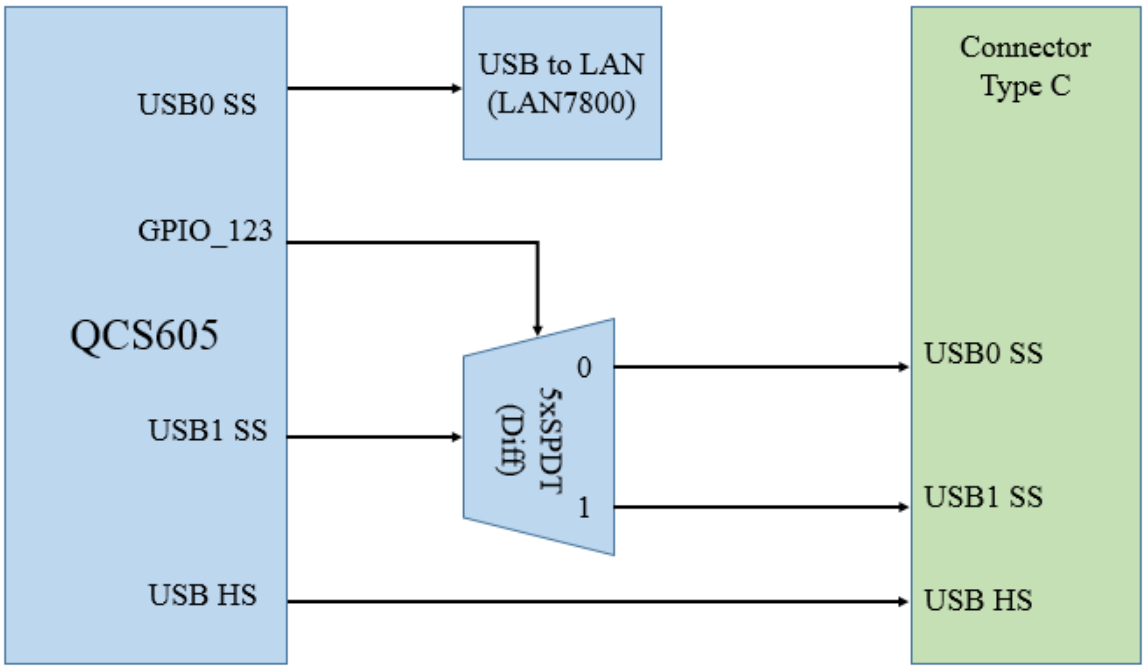

Figure 6. USB Port

The QCS605 processor includes two USB SS ports and one USB HS port:

- USB SS0 is for a normal host port.
- USB SS1 and USB HS are for a Type C port.

The board can work in one mode at a time, host mode or device mode, but not both.

3.9.1 USB host port

USB SS0 port is configured in host mode for USB to LAN function.

In this design, LAN7800 is used as a USB to LAN controller.

3.9.2 USB device port

The K200 Sub board implements a USB device port. The port is located at #2 (see Section 1.2.1), a Type C connector.

The Type C connector supports a device or host with different peripherals. The QCS605 processor configures the port based on Type C rules. Use a 2:1 muxing device with input of USB SS0 and USB SS1 from USB Type C, output directly to USB SS1 port of QCS605.

3.10 Audio

3.10.1 Line in and line out

The K200 Sub board supports one port 3.5 line in (see Section 1.2.1, #11) and one port 3.5 line out (see Section 1.2.1, #10) on the board.

3.10.2 Speaker amplifier

Integrated mono Class-D (1.2 W/5 V/8 Ω) and 1 PDM ports support for wsa881x Mono / Stereo WSA8810: 2.0 W / 6 V / 8 Ω or WSA8815: 4.0 W / 9.5 V / 8 Ω.

3.10.3 Digital Microphone

Support 2 Ports DMIC (4 x Digital Microphones) on QCS605.

3.10.4 HDMI audio

A 4-bit (audio out only) I2S channel is routed directly from the QCS605SoC I2S interface pins to the DSI-HDMI bridge

3.10.5 DisplayPort audio

The DisplayPort audio is routed directly from the QCS605SoC EDP interface pins to the Type C USB connector.

3.10.6 BT audio

The BT 5.0 implementation (including audio) on the K200 is with QCS605 and WCN3990.

3.11 DC and battery power

The K200 Sub board power is supplied in one of the following ways:

- Through a dedicated DC jack (5.5x2.1mm) by using 12V external adapter.
- Through a dedicated RJ45 jack by using 802.3af/at PoE-PSE.

See Section 6 for details on Sub board DC power implementation.

3.12 DC Power Measurements

By using some devices connected to Sub board, we can measure power consumption in some operation script of Sub board. See section 6.4 for details.

3.13 Button

There is one button in the K200 Sub board, used for power on/ off/ reset function.

3.14 LED

The K200 Sub board supports implementation of three LEDs on the board:

Two activity LEDs:

- One of the LEDs is an activity indicator of Ethernet block drives this Green LED via GPIO5 from the LAN7800.
- One of the LED is a speed indicator of Ethernet block drives this Green LED via GPIO6 from the LAN7800.

Power indicator LED

- A green LED is used to indicate the presence of input power.

3.15 UART

The K200 Sub board support one SoC UART interface directly from SoC pins to low-speed expansion connector J0805, UART_TX and UART_RX connect to pin 20 and 21 respectively.

3.16 Ethernet connector

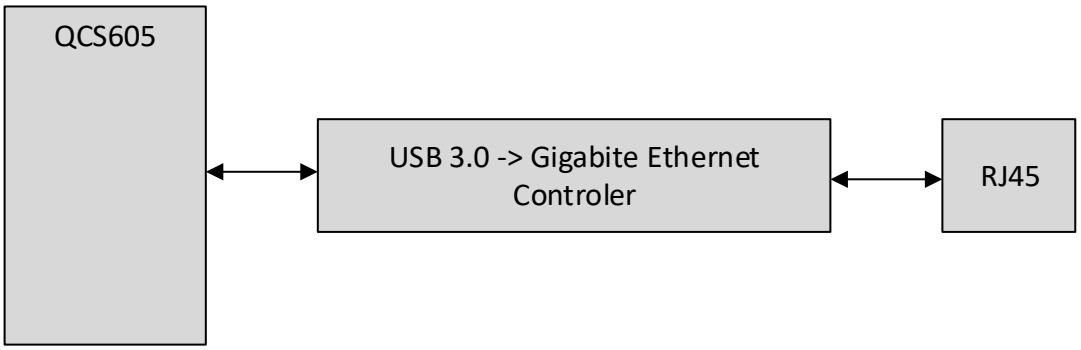

Figure 7. Ethernet connector

The K200 Sub board has the translation from USB 3.0 to Gigabit Ethernet controller. The K200 Sub board uses an RJ45 as the physical interface.

3.17 Expansion connector

The K200 Sub board specification calls for two expansion connector groups, low-speed connector and high-speed connector. See Section 4 for details about the low-speed expansion connector and Section 5 for details about the high speed expansion connectors.

4 Low-speed expansion connector

4.1 Low speed expansion 1, J0805

PIN	SOM Signal	SUB Signal
1	LPI_I2C_1_SDA	LPI_I2C_1_SDA
2	LPI_I2C_1_SCL	LPI_I2C_1_SCL
3	LPI_SPI_1_MISO_SNSR	LPI_SPI_1_MISO_SNSR
4	LPI_SPI_1_MOSI_SNSR	LPI_SPI_1_MOSI_SNSR
5	LPI_SPI_1_CLK_SNSR	LPI_SPI_1_CLK_SNSR
6	LPI_SPI_1_CS0_N_SNSR	LPI_SPI_1_CS0_N_SNSR
7	LPI_GPIO_6	LPI_GPIO_6
8	LPI_GPIO_7	LPI_GPIO_7
9	LPI_GPIO_8	LPI_GPIO_8
10	LPI_GPIO_9	LPI_GPIO_9
11	VREG_L10A_1P8	VREG_L10A_1P8
12	VREG_BOB_3P3	VREG_BOB_3P3
13	QCS605_GPIO_7	QCS605_GPIO_7
14	QCS605_GPIO_9	QCS605_GPIO_9

15	GND	GND
16	LPI_GPIO_14	LPI_GPIO_14
17	LPI_GPIO_15	LPI_GPIO_15
18	LPI_GPIO_16	LPI_GPIO_16
19	LPI_GPIO_17	LPI_GPIO_17
20	QUP12_UART_TX	QUP12_UART_TX
21	QUP12_UART_RX	QUP12_UART_RX
22	QUP10_I2C_SDA	QUP10_I2C_SDA
23	QUP10_I2C_SCL	QUP10_I2C_SCL
24	ACCL_GYRO_DRDY_INT	ACCL_GYRO_DRDY_INT
25	ACCL_GYRO_EVENT_INT	ACCL_GYRO_EVENT_INT
26	QCS605_GPIO_11	QCS605_GPIO_11
27	QCS605_GPIO_12	QCS605_GPIO_12
28	QCS605_GPIO_14	QCS605_GPIO_14
29	GND	GND
30	CBL_PWR_N	CBL_PWR_N

4.1.1 LPI GPIO

There are 16 LPI GPIOs in J0805 connector, all LPI GPIOs are routed from QCS605 SoC. The LPI GPIOs are 1.8V voltage rail.

4.1.2 UART

In this design, QUP12_UART_TX/RX are routed from QCS605SoC for debug.

- QUP12_UART_TX: Connect to GPIO_51 of QCS605 SoC.
- QUP12_UART_RX: Connect to GPIO_52 of QCS605 SoC.

4.1.3 I2C

The I2C interface is connected directly from QCS605SoC to device. In this design, use QUP10_I2C bus. A resistor is needed to provide pull-up for each of the I2C lines per I2C specification, the pull-ups are connected to 1.8V voltage rail in K200 board.

- QUP10_I2C_SDA: Connect to GPIO_55 of QCS605 SoC.
- QUP10_I2C_SCL: Connect to GPIO_56 of QCS605 SoC.

4.1.4 GPIO

There are 7 GPIOs in this connector, all GPIOs are routed from QCS605 SoC. The GPIOs are 1.8V voltage rail.

4.2 Low speed expansion 2, J0808

PIN	SOM Signal	SUB Signal
1	LPI_GPIO_10	LPI_GPIO_10
2	VREG_DBU1_1P125	VREG_DBU1_1P125

3	VREG_S1B_0P8	VREG_S1B_0P8
4	VREG_L10B_0P8	VREG_L10B_0P8
5	VREG_S3B_S4B_0P752	VREG_S3B_S4B_0P752
6	VREG_L9B_0P752	VREG_L9B_0P752
7	VREG_L5A_0P8	VREG_L5A_0P8
8	VREF_MSM	VREF_MSM
9	VREG_S6A_1P352	VREG_S6A_1P352
10	VREG_L9A_1P8	VREG_L9A_1P8
11	VREG_L6A_1P304	VREG_L6A_1P304
12	VREG_L19A_3P312	VREG_L19A_3P312
13	VREG_DBU2_S3A_1P125	VREG_DBU2_S3A_1P125
14	VREG_L1A_1P2	VREG_L1A_1P2
15	VREG_S5B_0P6	VREG_S5B_0P6
16	VREG_L1B_0P88	VREG_L1B_0P88
17	LPI_GPIO_11	LPI_GPIO_11
18	VREG_L7B_3P088	VREG_L7B_3P088
19	VREG_L4B_2P96	VREG_L4B_2P96
20	VREG_S5A_0P752	VREG_S5A_0P752

21	VREG_S1A_0P752	VREG_S1A_0P752
22	PHONE_ON_N	PHONE_ON_N
23	PON_OUT	PON_OUT
24	PON_RESET_N	PON_RESET_N
25	PS_HOLD	PS_HOLD
26	PMIC_RESIN_N	PMIC_RESIN_N
27	FAULT_N	FAULT_N
28	VDD_OUT_PT_5V	VDD_OUT_PT_5V
29	GNSS_ELNA_CTRL	GNSS_ELNA_CTRL
30	WCSS_PWR_REQ	WCSS_PWR_REQ

Connect all power sequencing signals from PMIC (PM670, PM670L) to J0808 for debugging. By the way, can use these powers to supply to some external components with suitable voltage and current parameters. Refer to QCS605 SOM datasheet for more informations related to voltage and current.

4.3 Low speed expansion 3, J0803

PIN	SOM Signal	SUB Signal
1	FORCED_USB_BOOT	FORCED_USB_BOOT
2	VREG_L13A_1P8	VREG_L13A_1P8
3	JTAG_SRST_N	JTAG_SRST_N

4	JTAG_TCK	JTAG_TCK
5	JTAG_TDI	JTAG_TDI
6	JTAG_TDO	JTAG_TDO
7	JTAG_TMS	JTAG_TMS
8	JTAG_TRST_N	JTAG_TRST_N

4.3.1 JTAG

Connect all 6 signals JTAG from QCS605 to J0803 connector for debugging and testing.

4.3.2 FORCED USB BOOT

Connect FORCED_USB_BOOT from GPIO_57 of QCS605 SoC and 1.8V voltage rail (VREG_L13A_1P8) to J0803 for boot configuration during development or factory production.

4.4 Low speed expansion 4, J0801

PIN	SOM Signal	SUB Signal
1	SDM_DMIC_DATA2	SDM_DMIC_DATA2
2	WSA_SWR_CLK	WSA_SWR_CLK
3	WSA_SWR_DATA	WSA_SWR_DATA
4	WSA_EN1	WSA_EN1
5	WSA_EN2	WSA_EN2

6	CDC_MIC_BIAS1	CDC_MIC_BIAS1
7	SPKR_P	SPKR_P
8	SPKR_M	SPKR_M
9	SDM_DMIC_CLK1	SDM_DMIC_CLK1
10	SDM_DMIC_DATA1	SDM_DMIC_DATA1
11	SDM_DMIC_CLK2	SDM_DMIC_CLK2
12	CDC_MIC_BIAS2	CDC_MIC_BIAS2

4.4.1 Audio LPI GPIO

Four LPI GPIO, LPI_GPIO_26, LPI_GPIO_27, LPI_GPIO_28, LPI_GPIO_29 are used for DMIC 1 and DMIC 2 respectively. One MIC need two signal are DATA and CLOCK.

4.4.2 Audio GPIO

GPIO_65 is used for SoundWire clock, WSA_SWR_CLK

GPIO_66 is used for SoundWirel data, WSA_SWR_DATA

GPIO_67 is used to enable WSA1, WSA_EN1

GPIO_68 is used to enable WSA2, WSA_EN2

4.4.3 Audio Codec

Four signal are routed from PM670L to expansion connector to support 2 MIC and 1 speaker, they are CDC_MIC_BIAS1, CDC_MIC_BIAS2, SPKR_P, SPKR_M, respectively.

4.5 Low speed expansion 5, J0804

PIN	SOM Signal	SUB Signal
1	ALARM_IN_1+	ALARM_IN_1+
2	ALARM_IN_1-	ALARM_IN_1-
3	ALARM_IN_2+	ALARM_IN_2+
4	ALARM_IN_2-	ALARM_IN_2-
5	ALARM_OUT_A	ALARM_OUT_A
6	ALARM_OUT_B	ALARM_OUT_B

This connector is dedicated for ALARM I/O function. There are 2 Alarm Input and 1 Alarm Output as requirement.

- ALARM_IN_1+/-: for Alarm Input 1.
- ALARM_IN_2+/-: for Alarm Input 2.
- ALARM_OUT_A/B: for Alarm Output.

5 High-speed expansion connector

5.1 High speed expansion 1, J0809

PIN	SOM Signal	SUB Signal
1	GND	GND
2	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P
3	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N
4	GND	GND
5	MIPI_DSI1_LN0_P	MIPI_DSI1_LN0_P
6	MIPI_DSI1_LN0_N	MIPI_DSI1_LN0_N
7	GND	GND
8	MIPI_DSI1_LN1_P	MIPI_DSI1_LN1_P
9	MIPI_DSI1_LN1_N	MIPI_DSI1_LN1_N
10	GND	GND
11	MIPI_DSI1_LN2_P	MIPI_DSI1_LN2_P
12	MIPI_DSI1_LN2_N	MIPI_DSI1_LN2_N
13	GND	GND
14	MIPI_DSI1_LN3_P	MIPI_DSI1_LN3_P

15	MIPI_DSI1_LN3_N	MIPI_DSI1_LN3_N
16	GND	GND

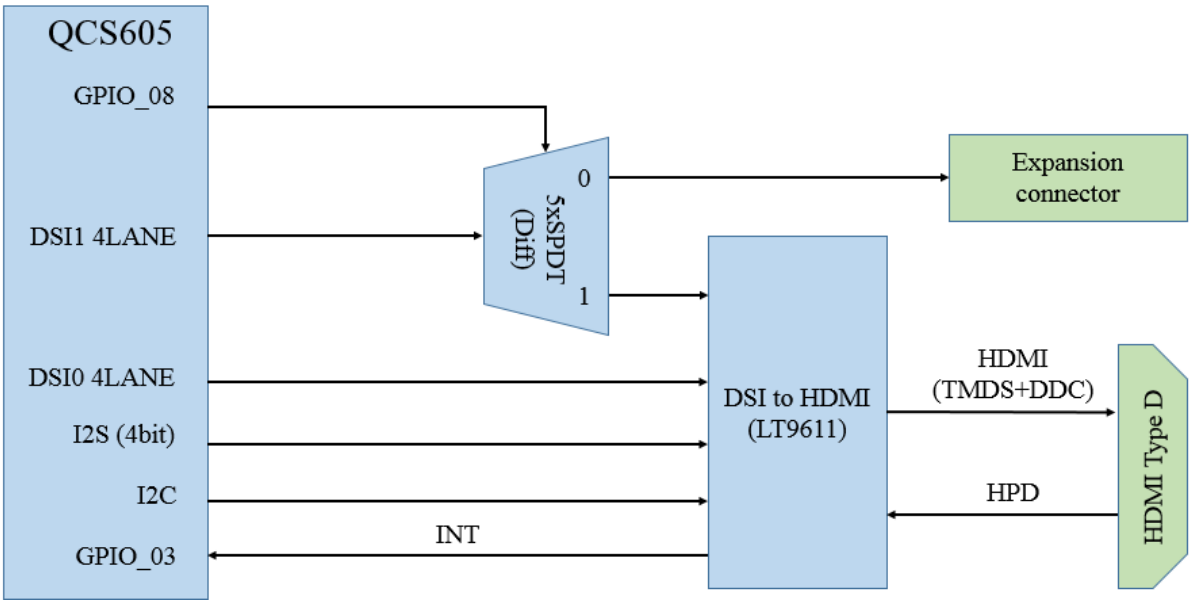

Figure 8. High speed expansion 1, J0809

The specification calls for a MIPI-DSI to be present on the high-speed expansion connector. A minimum of one lane is required and up to four lanes can be accommodated on the connector. The SUB board implementation supports a full 4-lane MIPI-DSI interface that is routed to the primary high-speed expansion connector. Since the QCS605 processor has no HDMI interface, and it is used to drive the DSI-HDMI bridge, DSI muxing is required. A muxing device (FSA644UCX) is used on the board. Only one interface, HDMI, or the expansion MIPI-DSI, can be active at a given time. The signal is named QCS605_GPIO_8. When this signal is logic level high, 1, the MIPI-DSI is routed to the DSI-HDMI bridge. When QCS605_GPIO_8 is logic level low, 0, the MIPI-DSI is routed to the high-speed expansion connector. This design assign the QCS605_GPIO_8 function to GPIO_8.

5.2 High speed expansion 2, J0901

PIN	SOM Signal	SUB Signal
1	QUP15_SPI_MISO	QUP15_SPI_MISO
2	QUP15_SPI_MOSI	QUP15_SPI_MOSI
3	QUP15_SPI_CLK	QUP15_SPI_CLK
4	QUP15_SPI_CS_N	QUP15_SPI_CS_N
5	ZOOM_FOCUS_IRIS_RESET	ZOOM_FOCUS_IRIS_RESET
6	ZOOM_FOCUS_IRIS_BUSY	ZOOM_FOCUS_IRIS_BUSY
7	ZOOM_FOCUS_IRIS_VSYNC1	ZOOM_FOCUS_IRIS_VSYNC1
8	ZOOM_FOCUS_IRIS_VSYNC2	ZOOM_FOCUS_IRIS_VSYNC2
9	AVDD_CAM_2P9	AVDD_CAM_2P9
10	AVDD_CAM_2P9	AVDD_CAM_2P9
11	GND	GND
12	GND	GND
13	DVDD_CAM_1P2	DVDD_CAM_1P2
14	DVDD_CAM_1P2	DVDD_CAM_1P2
15	GND	GND
16	GND	GND

17	GND	GND
18	MIPI_CSI0_DLN3_P_CONN	MIPI_CSI0_DLN3_P_CONN
19	MIPI_CSI0_DLN3_N_CONN	MIPI_CSI0_DLN3_N_CONN
20	GND	GND
21	MIPI_CSI0_DLN1_N_CONN	MIPI_CSI0_DLN1_N_CONN
22	MIPI_CSI0_DLN1_P_CONN	MIPI_CSI0_DLN1_P_CONN
23	GND	GND
24	MIPI_CSI0_DCLK_P_CONN	MIPI_CSI0_DCLK_P_CONN
25	MIPI_CSI0_DCLK_N_CONN	MIPI_CSI0_DCLK_N_CONN
26	GND	GND
27	MIPI_CSI0_DLN0_P_CONN	MIPI_CSI0_DLN0_P_CONN
28	MIPI_CSI0_DLN0_N_CONN	MIPI_CSI0_DLN0_N_CONN
29	GND	GND
30	MIPI_CSI0_DLN2_N_CONN	MIPI_CSI0_DLN2_N_CONN
31	MIPI_CSI0_DLN2_P_CONN	MIPI_CSI0_DLN2_P_CONN
32	GND	GND
33	GND	GND
34	GND	GND

35	VREG_CAM_3P3	VREG_CAM_3P3
36	CAM_MCLK0	CAM_MCLK0
37	CAM0_RST_N	CAM0_RST_N
38	GND	GND
39	GND	GND
40	VREG_CAM_3P3	VREG_CAM_3P3
41	VREG_CAM_3P3	VREG_CAM_3P3
42	VDD_OUT_PT_5V	VDD_OUT_PT_5V
43	VDD_OUT_PT_5V	VDD_OUT_PT_5V
44	OVDD_CAM_1P8	OVDD_CAM_1P8
45	GND	GND
46	GND	GND
47	IRCUT_INA	IRCUT_INA
48	IRCUT_INB	IRCUT_INB
49	CCI_I2C_SCL0	CCI_I2C_SCL0
50	CCI_I2C_SDA0	CCI_I2C_SDA0

5.2.1 CAM MCLK

The K200 Sub board implement one CSI clock, CAM_MCLK0 via QCS GPIO_13, this signal is driven at 1.8V.

5.2.2 CAM CCI I2C

The K200 Sub board implement one I2C interface for camera function, CCI_I2C_SCL0 and CCI_I2C_SDA0 are routed from GPIO_17 and GPIO_18 of QCS605 respectively. I2C interface have an onboard 2.2K pull-up resistor pulled-up to the 1.8V voltage rail.

5.2.3 CAM CSI0

The K200 Sub board implementation support a full 4-lane MIPI-CSI interface on CSI0, is routed directly to and from the QCS605 processor.

5.2.4 CAM GPIO

Some GPIOs are routed directly from QCS605 to K200 Sub board for SPI,Zoom/ Focus/ Iris, IR CUT functions respectively.

QUP15_SPI_MISO, QUP15_SPI_MOSI , QUP15_SPI_CLK , QUP15_SPI_CS_N are routed from GPIO_81, GPIO_82, GPIO_83, GPIO_84 of QCS605 respectively. These GPIOs are SPI interface pins, used for comunication between QCS605 and

LC898201TA-NH driver IC on Image sensor board.

Besides, ZOOM_FOCUS_IRIS_BUSY signal is connected to GPIO_109, send busy signal to QCS605.

LC898201TA-NH is the appropriate motor control IC for the surveillance camera usage, and it can drive Iris, Focus, Zoom and Day/Night switching simultaneously.

ZOOM_FOCUS_IRIS_RESET, ZOOM_FOCUS_IRIS_VSYNC1, ZOOM_FOCUS_IRIS_VSYNC2 are routed from GPIO_112 , GPIO_94, GPIO_95 of QCS605 respectively. These GPIOs control LC898201TA-NH such as reset and

synchronization. QCS605 controls the IR Cut block through GPIO_107 (IRCUT_INA) and GPIO_110 (IRCUT_INB).

5.2.5 CAM Power supply

The KIT specification call for IMX327 image sensor, three power rails DVDD_CAM_1P2, AVDD_CAM_2P9, OVDD_CAM_1P8 are used for digital core, analog core, interface core of IMX327 respectively.

By the way, two other power rails VREG_CAM_3P3 and VDD_OUT_PT_5V are used for IR CUT function in lens module.

5.3 High speed expansion 3, J0807

PIN	SOM Signal	SUB Signal	Note
1	GND	GND	
2	MIPI_CSI1_DLN3_P	MIPI_CSI1_DLN3_P	
3	MIPI_CSI1_DLN3_N	MIPI_CSI1_DLN3_N	
4	GND	GND	
5	MIPI_CSI1_DLN2_P	MIPI_CSI1_DLN2_P	
6	MIPI_CSI1_DLN2_N	MIPI_CSI1_DLN2_N	
7	GND	GND	
8	MIPI_CSI1_DLN1_P	MIPI_CSI1_DLN1_P	
9	MIPI_CSI1_DLN1_N	MIPI_CSI1_DLN1_N	
10	GND	GND	

11	MIPI_CSI1_DLN0_P	MIPI_CSI1_DLN0_P	
12	MIPI_CSI1_DLN0_N	MIPI_CSI1_DLN0_N	
13	GND	GND	
14	MIPI_CSI1_DCLK_P	MIPI_CSI1_DCLK_P	
15	MIPI_CSI1_DCLK_N	MIPI_CSI1_DCLK_N	
16	GND	GND	

5.4 High speed expansion 4, J0806

PIN	SOM Signal	SUB Signal	Note
1	GND	GND	
2	MIPI_CSI2_DCLK_P	MIPI_CSI2_DCLK_P	
3	MIPI_CSI2_DCLK_N	MIPI_CSI2_DCLK_N	
4	GND	GND	
5	MIPI_CSI2_DLN0_P	MIPI_CSI2_DLN0_P	
6	MIPI_CSI2_DLN0_N	MIPI_CSI2_DLN0_N	
7	GND	GND	
8	MIPI_CSI2_DLN1_P	MIPI_CSI2_DLN1_P	
9	MIPI_CSI2_DLN1_N	MIPI_CSI2_DLN1_N	

10	GND	GND	
11	MIPI_CSI2_DLN2_P	MIPI_CSI2_DLN2_P	
12	MIPI_CSI2_DLN2_N	MIPI_CSI2_DLN2_N	
13	GND	GND	
14	MIPI_CSI2_DLN3_P	MIPI_CSI2_DLN3_P	
15	MIPI_CSI2_DLN3_N	MIPI_CSI2_DLN3_N	
16	GND	GND	

The specification calls for two MIPI-CSI interfaces to be present on the high-speed expansion connector (J0806, J0807). Both interfaces are optional. Both CSI1 and CSI2 interfaces can be up to four lanes. All MIPI-CSI signals are routed directly to and from the QCS605 processor.

6 Power management

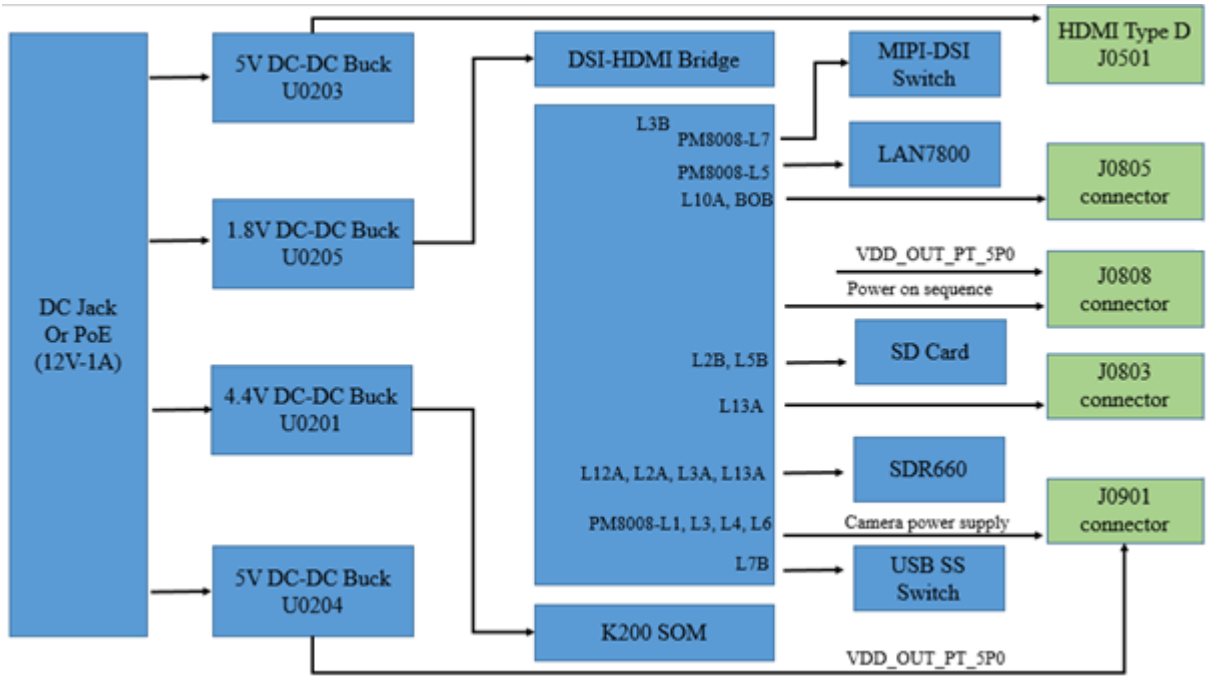

Figure 9. Power management

In this section, the power supply scheme for all units on KIT will be detailed.

In addition to using Qualcomm-based PMIC solutions on the SOM circuit (refer to the power supply scheme on the SOM circuit in the datasheet document), some of those DC-DC converters are also used on the SUB circuit was:

- U0201: Buck type converter, generating 4.4V of voltage, maximum current of 3A, supplying VBATT_PWR to PM670 power on the SOM circuit.
- U0203: Buck type converter, generating 5V voltage, maximum current of 3A, powering DSI to HDMI converter unit.
- U0204: Buck type converter, generating 5V voltage, maximum current of 3A, supplying power to LEN control unit, supplying to J0805 connector.

- U0205: LDO type converter, generating 1.8V voltage, maximum current 0.8A, powering DSI to HDMI converter unit.

6.1 DC power input

For the input power supply, the KIT can be powered in one of two ways as follows:

- 12V power supply via DC Jack - J1004
- Standard 802.3at/af PoE power supply via RJ45 Jack - J1202

At this design, PoE-PD module is used with input from RJ45 connector or DC Jack, output of module is 12V DC which is used to power to system.

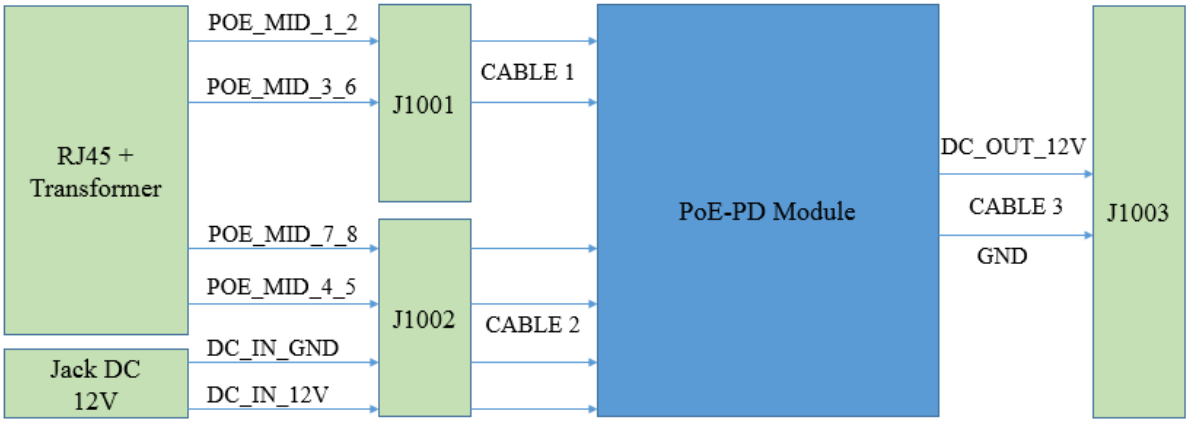

Figure 10. DC power input

6.2 Power source selection

As shown in section 6.1, the device can be powered in one of two ways. The device only accepts one of the two types of power supply at a time. The choice of the type of feed depends on the needs and actual conditions of the user.

6.3 Power sequencing

After the device is powered from one of the two ways above, the U0201 will be powered on and convert the input 12V source to a 4.4V, through 1 overcurrent protection IC, this

4.4 power will be supplied to VBATT pins of PM670 ready to feed the entire system. After having the trigger signal, starting the power-on sequence PMIC will turn on all sources in the correct power - on sequence.

7 Button and status LEDs

7.1 Power Button

The push-button (see Section 1.2.1, #22) serves as the power ON/OFF/Sleep button. Upon applying power to the board, the boot process will start. Once the board is powered on and booted up.

7.2 LEDs

Refer to Section 3.13

8 Boot configuration

Some signals in expansion connector J0802, J0803, J0808 can used to configure boot scenarios, as below:

- J0802 – Pin 13, CBL_PWR_N: When set to ON, will force the device to boot up automatically; when set to OFF, will force the device to boot up by manual power button.
- J0803 – Pin 1, FORCED_USB_BOOT: When connect to Pin 2, VREG_L13A_1P8, will force the device to QDL Mode.
- J0808 – Pin 26, PMIC_RESIN_N: When set to ON, will force the device to fast boot.

9 Mechanical specification

Top view

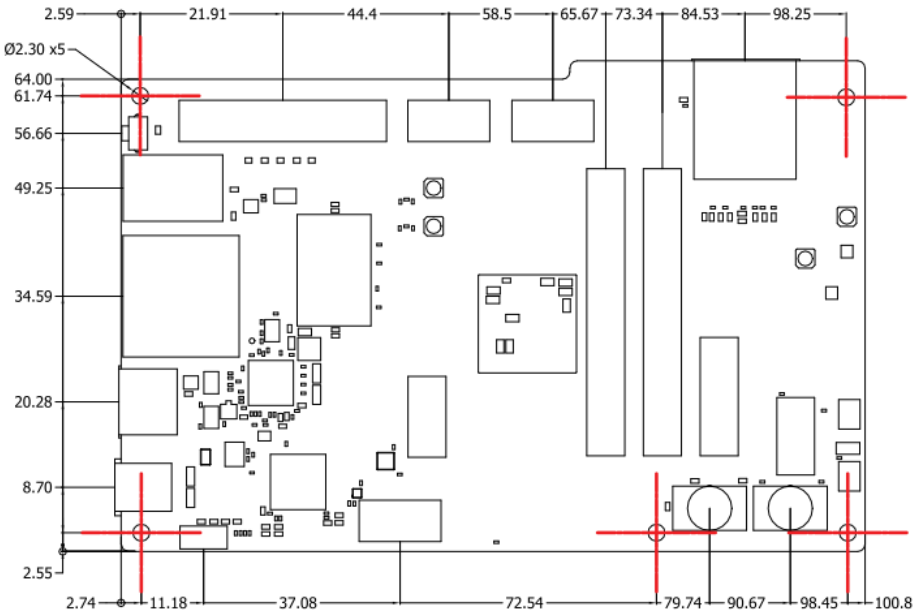

Figure 11. Mechanical Top view

Bottom view

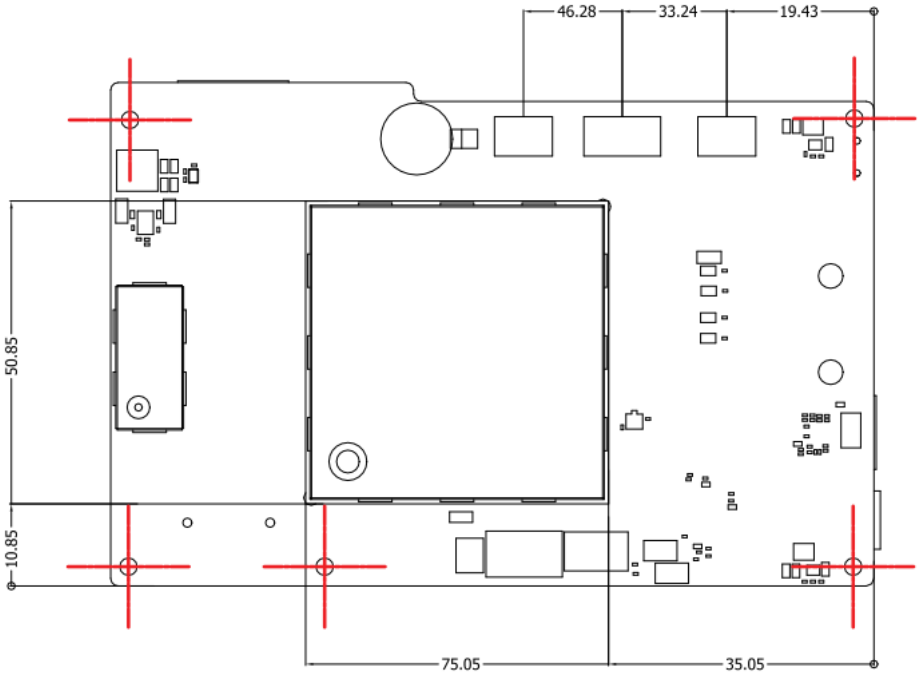

Figure 11. Mechanical Top view